AMENDMENTS TO CLAIMS

Please amend claims as follows.

1. (currently amended) A method of manufacturing a semiconductor device, comprising the steps of:

providing a substrate;

forming a mask layer over the substrate;

patterning the mask layer and the substrate to form a first opening in the substrate;

forming a gate dielectric layer~~, a first conductive layer~~ and a polycide ~~second conductive~~ layer inside the first opening sequentially, wherein the ~~gate dielectric layer covers the interior surface of the first opening, the first conductive layer covers the gate dielectric layer and the second conductive~~ polycide layer ~~completely~~ fills the first opening;

removing a portion of the ~~first conductive layer and the second conductive~~ polycide layer so that ~~the~~ an upper surface of a ~~remaining first conductive layer and a remaining second conductive~~ remainder polycide layer in the first opening ~~are~~ is at a level slightly below ~~the~~ an upper surface of the substrate and thereby form a second opening;

forming a cap layer inside the second opening;

removing the mask layer; and

forming a source/drain region in the substrate.

2. (original) The method of claim 1, wherein the step of forming the source/drain region is performed after the step of removing the mask layer.

3. (original) The method of claim 1, wherein the step of forming the source/drain region in the substrate is performed before the step of forming the mask layer over the substrate.

4. (original) The method of claim 3, further comprises a step of forming a well region in the substrate before the step of forming source/drain region in the substrate.

5. (original) The method of claim 4, wherein the step of forming the source/drain region and the step of forming the well region in the substrate use the same layer as a implanting mask.

6. (original) The method of claim 1, further comprises a step of forming a well region in the substrate before the step of forming the mask layer on the substrate.

7. (original) The method of claim 1, wherein after the step of forming a mask layer over the substrate, furthermore comprises forming a bottom anti-reflection layer over the mask layer; and the step of patterning the mask layer and the substrate to form a first opening furthermore comprises patterning the bottom anti-reflection layer.

Claim 8 (canceled).

9. (currently amended) The method of claim 1, wherein the polycide ~~second conductive~~ layer comprises a polysilicon layer and a refractory metal silicide layer.

10. (currently amended) The method of claim 9, wherein a material constituting the refractory metal silicide layer is selected from a group consisting of tungsten silicide,

nickel silicide, cobalt silicide, titanium silicide, molybdenum silicide, platinum silicide and palladium silicide.

11. (currently amended) The method of claim 1, wherein the step of removing a portion of the ~~first conductive layer and the second conductive~~ polycide layer comprises:

performing a chemical-mechanical polishing process to remove a portion ~~portions of the first conductive layer and the second conductive~~ polycide layer outside the first opening; and

etching back the remainder polycide ~~first conductive layer and the second conductive~~ layer in the first opening ~~so that the~~ until an upper surface of ~~the~~ a remaining polycide ~~first conductive layer and the remaining second conductive~~ layer in the first opening are at a level slightly below the upper surface of the substrate and thereby form a second opening.

12. (original) The method of claim 1, wherein the mask layer is fabricated using a material having an etching selectivity that differs from the material constituting the first conductive layer, the second conductive layer and the cap layer.

13. (currently amended) The method of claim 1, wherein after the step of patterning the mask layer and the substrate to form the first opening further comprises performing a threshold voltage adjustment process.

14. (original) The method of claim 1, further comprising:

forming an inter-layer dielectric layer over the substrate; and

forming a contact opening in the inter-layer dielectric layer using the cap layer as a self-aligned mask.

Claims 15-23 (canceled).

24. (new) A method of manufacturing a semiconductor device, comprising the steps of:

forming an opening in a substrate;

forming a doped polysilicon layer over the sidewalls of the opening; and

forming a polycide layer over the doped polysilicon layer inside the opening such that an upper surface of the polycide layer is lower than a top surface of the substrate, wherein sidewalls of the polycide layer is enclosed by the doped polysilicon layer.

25. (new) The method of claim 24, wherein the polycide layer comprises a polysilicon layer and a refractory metal silicide layer.

26. (new) The method of claim 25, wherein a material constituting the refractory metal silicide layer is selected from a group consisting of tungsten silicide, nickel silicide, cobalt silicide, titanium silicide, molybdenum silicide, platinum silicide and palladium silicide.

27. (new) The method of claim 1, wherein the step of forming the polycide layer comprises:

sequentially forming a polysilicon layer and a refractory metal silicide layer over the doped polysilicon layer and filling the opening;

performing a chemical-mechanical polishing process to remove portions of the polysilicon layer and the refractory metal silicide layer outside the opening; and

etching back the remainder portions of the polysilicon layer and the refractory metal silicide layer in the opening until an upper surface of a remaining portions the polysilicon layer and the refractory metal silicide layer in the opening layer in the opening are at a level below the upper surface of the substrate.